REMARKS

The Office Action dated August 6, 2008 has been received. In this response, new claims 55-57 have been added. Reconsideration of the outstanding rejection in the present application is respectfully requested based on the following remarks.

Obviousness Rejection of Claims 13, 15-29, 31-40, 43-50, and 52-54

At page 2 of the Office Action, claims 13, 15-29, 31-40, 43-50, and 52-54 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eifrig (U.S. Patent No. 6,748,020) in view of Pian (U.S. Patent No. 6,366,614). This rejection is respectfully traversed.

Independent claim 13 recites the features of a decoder instruction packet (DIP) sequencer to access one or more packets of the plurality of packets from the memory via the memory controller and configure the second processor based on opcodes of the one or more packets. Similarly, independent claim 44 recites the features of a decoder instruction packet (DIP) sequencer to access from the memory via the memory controller one or more packets and configure a first processor based on opcodes of the one or more packets" and independent claim 53 recites the features of accessing the one or more packets from the memory via a decoder instruction packet (DIP) sequencer and configuring, via the DIP sequencer, the second processor based on opcodes of the one or more packets. Thus, each of independent claims 13, 44, and 53 provides that one of two recited processors of the claim is configured via a DIP sequencer based on opcodes of one or more packets accessed from memory by the DIP sequencer.

With respect to the claimed aspects of configuring a processor via the DIP sequencer based on one or more packets, the Office asserts "Eifrig et al discloses . . . a decoder instruction packet (DIP) sequencer to access one or more packets from the one or more packets; and provide the one or more packets to the second processor for transcoding (fig. 3b, el. 50 and col. 8, lines 6-14, 34-36) as specified in claim 13." *Office Action*, p. 2. The Office further relies on the cited passages of Eifrig at FIG. 3b, element 50 and col. 8, lines 6-14 and 34-36 in rejecting the above-identified aspects of claims 44 and 53. *Id.*, p. 4. Turning to these relied-upon passages, FIG. 3b of Eifrig (reproduced below) illustrates "a Transcoder Processing Element (TPE) software architecture" (Eifrig, col. 7, lines 62-65) that includes a scheduler 350.

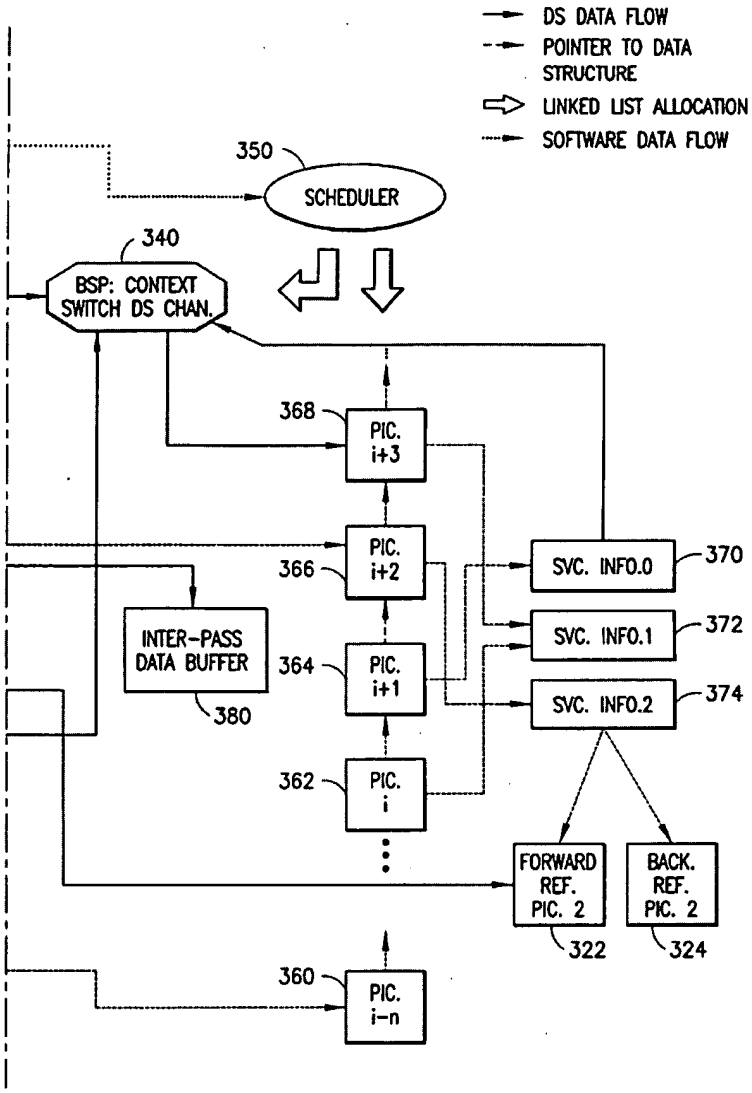

FIG.3b

The cited passages of Eifrig at col. 8, lines 6-14 and 34-36 teach:

> A transport channel input 308 is demultiplexed (at a demux 306) to provide the three data services to respective input rate buffers 310, 312 and 314. The data services are decoded in turn at a variable length decoder 304, which is responsive to a BSP context switch DS channel function 340, which is, in turn, responsive to a scheduler 350 and service information 370, 372 and 374 of the respective services.
>
> ...
>
> Processing of a number of pictures i-n (360), . . . , i (362), i+1 (364), i+2 (366), i+3 (368) is controlled by the scheduler 350.

However, neither FIG. 3b of Eifrig nor the above-reproduced passages of Eifrig disclose or render obvious that the scheduler 350 (alleged as the claimed DIP sequencer) configures a processor based on one or more packets obtained from a memory as provided by claims 13, 44, and 53. Rather, these passages merely teach that processing of pictures is *controlled* by the scheduler 350. Controlling the processing of pictures is not the same as, or even equivalent to, configuring a processor based on one or more packets as provided by the claims, and the Office has not provided any evidence or rationale to the contrary. In fact, other than citing the above-identified passages of Eifrig, no explanation of how Eifrig teaches a DIP scheduler to configure a processor based on one or more packets accessed from memory by the DIP scheduler. Thus, the Office fails to establish a *prima facie* case of obviousness for at least this reasons.

Accordingly, contrary to the assertions of the Office, Eifrig fails to disclose or render obvious the above-identified claim features. The Office relies on Pian merely to support a theory that implementing the features of the claims in two separate processors as provided by the claims would be obvious. *Office Action*, pp. 6-7. The Office does not assert that Pian discloses the above-identified claim features, nor does Pian in fact disclose or render obvious these claim features.

Moreover, independent claims 13, 44, and 53 recite subject matter directed to a first processor and a second processor and their respective functionality/operations. For each of claims 13, 44, and 53, the Office asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the claimed "first processor" feature and that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the claimed "second processor" feature. *See Office Action*, pp. 2, 4, and 6. As discussed in greater detail at pages 9-12 of the Response filed May 7, 2007 (hereinafter, "the First Response") and at pages 9-11 of the Response filed November 20, 2007 (hereinafter, "the Second Response"), and as acknowledged by the Office at page 6 of the Office Action, Eifrig fails to disclose that element 10 and element 30 are implemented as separate processors. In fact, Eifrig expressly teaches that element 10 and element 30 are implemented at the same Very Long Instruction Word (VLIW) core. *See, e.g., Eifrig*, col. 4, lines 6-33 ("a) MPEG transport stream decoding (on VLIW core)(10) [. . .] c) Core transcoding (on VLIW core)(30) [. . .]")(emphasis added). As also discussed in the First Response and the Second Response, one of ordinary skill in the art will recognize that the parsing/demux (element 10) and

the corresponding core transcoder (element 30) conventionally are implemented together as a single processor.

The Office responds to the failure of Eifrig to contemplate separate processors by turning to Pian, which the Office alleges as teaching "in figure 1, elements 10 and 12, that a preprocessor and an encoder can be constructed as two separate processors. And, therefore, it would have been obvious . . . to modify the system of Eifrig et al by constructing a preprocessor and [a] transcoder as two separate processors as taught by Pian et al as a matter of various variance [sic] . . ." *Office Action*, p. 7. Contrary to the Office's assertions, nowhere does Pian disclose or suggest that the preprocessor 10 and the encoder 12 are constructed as separate processors. For example, while the preprocessor 10 and the encoder 12 as represented in FIG. 1 of Pian using different boxes, nowhere does Pian attribute any particular meaning to this use of different boxes as being associated with separate processors, and one of ordinary skill in the art would correctly interpret the use of different boxes for the preprocessor 10 and the encoder 12 merely as a common format for partitioning the different functions provided by each. Further, at the passage at col. 4, lines 38-42, Pian teaches that the "encoder 12 and rate controller 14[] are implemented in a microprocessor or digital signal processor programmed to provide the functions as described" but fails to disclose or even suggest that the preprocessor 10 is implemented in a second processor separate from the "microprocessor or digital signal processor" in which the encoder 12 is implemented. Thus, as neither Eifrig nor Pian discloses or suggests separate processors, the combination of Eifrig and Pain fails to disclose or suggest separate processors.

As explained above, the proposed combination of Eifrig and Pian fails to disclose or render obvious each and every feature recited by claims 13, 44, and 53, as well as the particular combinations of features recited by claims 15-29, 31-40, 43, 45-50, 52, and 54 at least by virtue of their respective dependencies from one of claims 13, 44, and 53. Moreover, these claims recite additional novel features.

In view of the foregoing, reconsideration and withdrawal of the obviousness rejection is respectfully requested.

New Claims 55-57

New claims 55-57 have been added. New claim 55 depends from claim 53 and recites the additional features of "wherein a format of the one of more packets is independent of a video standard of the data stream." New dependent claims 56 and 57 depend from claims 13 and 44, respectively, and recite similar features. Support for the addition of the new claims is found in the Present Application as originally filed (*see, e.g., Present Application*, p. 19, lines 3-9). New claims 55-57 are allowable over the cited references at least by virtue of their respective dependencies from claims 53, 13, and 44. Moreover, none of the cited references disclose or render obvious the additional features recited by new claims 55-57.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Applicants believe no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-1835.

Respectfully submitted,

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